

# 長庚大學九十七學年度研究所碩士班(含在職專班)招生考試試題

所別：電機工程所碩士班

考試科目：邏輯設計

注意：請詳細閱讀下列試題，並請標明題號依試題順序將答案書寫於答案卷上。 本分試題共計 1 頁

- Explain the following network topologies commonly used in the local area network (LAN) by (A) drawing simple diagrams (for example, link-node representation) and (B) state the features advantages/ disadvantages respectively: (1) Ring; (2) Star; (3) Chained (or so-called line); (4) Line; (5) Tree (or so-called hierarchical). (3 % for each).
- Design a 4-bit priority encoder as the block diagram shown in Fig. 1. In this diagram,  $x$  is the most significant bit (MSB) and  $y$  is the least significant bit (LSB), and note that  $P_i$  has higher priority than  $P_j$  if  $i > j$ .  
 (A) Find the truth table; (10%)  
 (B) Draw the logic diagram layout you designed. (10%)
- You are required to design a logic circuit to control the lighting of two LCD segments  $P$  and  $Q$  in a display indicator as shown in the following block diagram as shown in Fig. 2. Each segment lights up when the control line ( $p$  or  $q$ ) is 0 (not 1).  $A_1, A_0, B_1,$  and  $B_0$  are binary-digit inputs. When  $p = A_1A_0 > B_1B_0 = q$ , the display will light up as “+”. On the contrary, when  $p < q$ , the display will light up as “-”. And when  $p = q$ , the display does not light up.  
 (A) Derive the simplified Boolean function for each of the control lines  $p$  and  $q$  in the “sum-of-product” form; (10%)  
 (B) Draw the logic circuit diagram you design. (10%)
- Determine the computational complexity of the following codes: ( 5 % for each)

(A) for  $i = 1$  to  $n$  do  
 for  $j = 1$  to  $n$  do  
 for  $k = 1$  to  $n$  do  
 $x = x + 1$ ;  
 end;  
 end;  
 end;

(B)  $i = 1$ ;  
 while  $i \leq n$  do  
 $x = x + 1$ ;  
 $i = i + 1$ ;  
 end;

(C) for  $i = 1$  to  $n$  do  
 $j = 1$ ;  
 for  $k = j + 1$  to  $n$  do  
 $x = x + 1$ ;  
 end;  
 end;

(D)  $k = 100000$ ;  
 while  $k \neq 5$  do  
 $k = k \text{ div } 10$ ;  
 end;

- Suppose there is an 8-bit central processing unit (CPU) with 16 address lines, please use AND/OR gates to enable four 16K-byte RAM modules. The address of the RAM must be continuous. Figure 3 shows the diagram of the CPU and RAM units (Where ADD = address, RD = read, WR = write, EN = enable).  
 (A) Write down in detail of the addressing/ data bus-line number and the arrangement of the used RAM and CPU; (5 %)  
 (B) Draw the circuit diagram of your design. (10 %)
- Implement the following Boolean function with the programmable logic array (PLA) configuration: (10%)

$$f_1 = \overline{A}B + AC + \overline{A}\overline{B}\overline{C} \quad \text{and} \quad \overline{f_2} = AC + BC$$

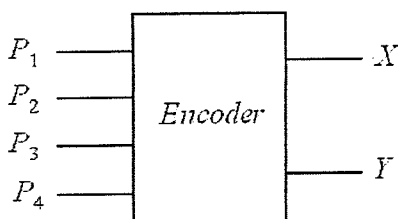


Fig. 1

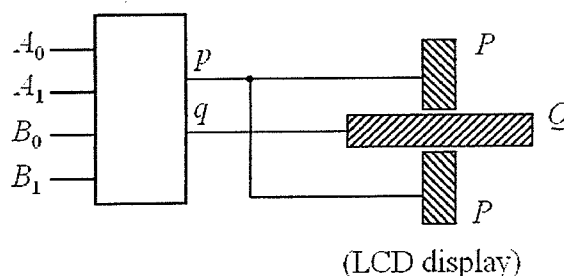


Fig. 2.

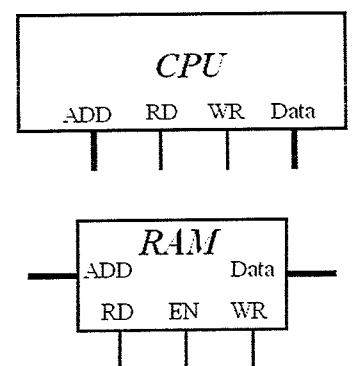


Fig. 3.